HyperTransport™ Technology Overview & Consortium Announcement

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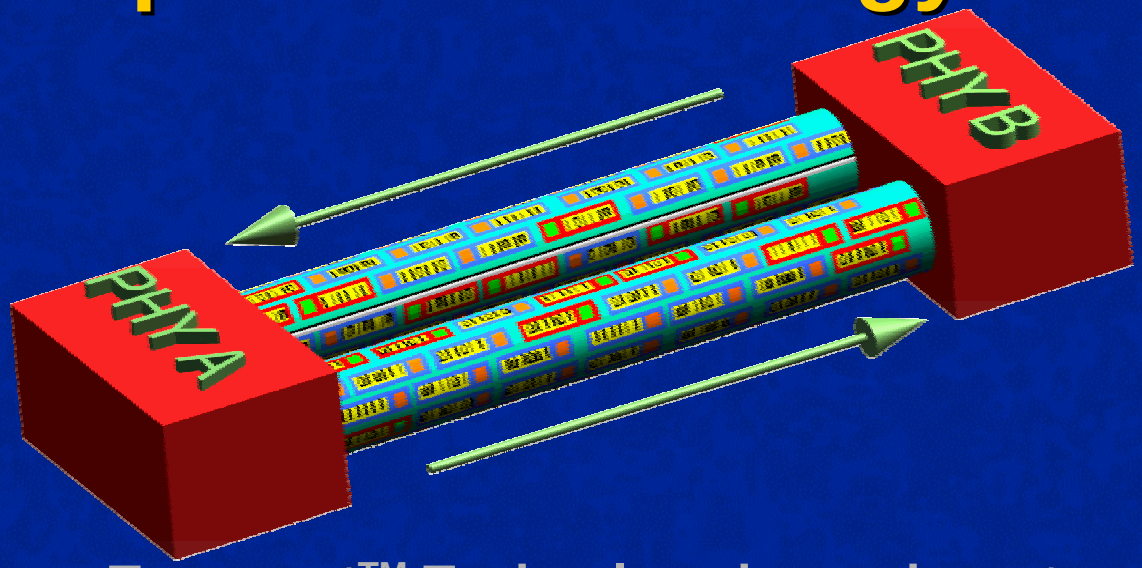
HyperTransport CONSORTIUM

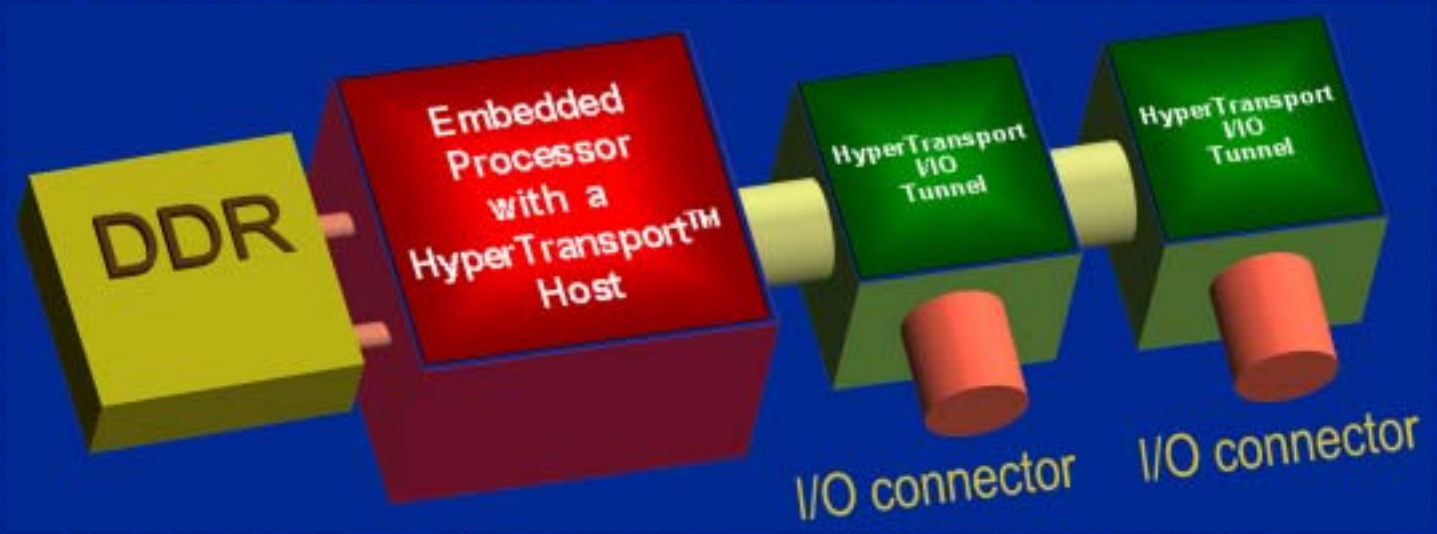
Platform Conference
Direction • Design • Perspective • Analysis

HyperTransport™ Technology Basics



- **HyperTransport™ Technology buses have two unidirectional point-to-point links**
  - The links can be 2-, 4-, 8-, 16-, or 32-bits wide in each direction
  - HyperTransport links have a data rate up to 1600 Megabits/second per pin-pair (800 MHz clock)
    - **E.g., 4 bits each way give up to 1.6 GB/sec total bandwidth**
    - **E.g., 8 bits each way give up to 3.2 GB/sec total bandwidth**
    - **E.g., 16 bits each way give up to 6.4 GB/sec total bandwidth**
    - **E.g., 32 bits each way give up to 12.8 GB/sec total bandwidth**
- **Packets are multiples of 4-bytes in length**
- **Serial link with commands, addresses and data use the same bits**

Embedded Applications and I/O Tunnels



- **For the 1st time in the industry:**
  - I/O devices shared among computation and communication industry
  - Unique “TUNNELING” capability gives almost unlimited I/O expandability
  - Fundamentally different microprocessor and memory controllers may be designed to use the very same I/O components
  - Pin count adjustable for the necessary Bandwidth
  - Cost reduced due the the cumulative volume
  - Extended component life

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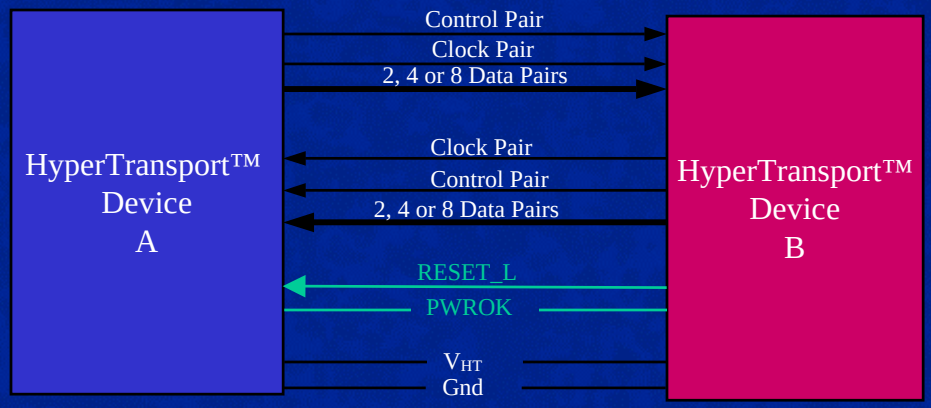
HyperTransport™ Device Pin Count

- **Additional HyperTransport™ Device signals**
  - Power OK (PWROK)
  - Reset HyperTransport Device (RESET_L)
- **55-pin HyperTransport device bus provides 12X the bandwidth of PCI-32/33 with fewer pins**
- **Signal to ground ratio is designed to be 4:1**
- **Optional link power down signals for mobile systems**
  - HyperTransport Device Stop_L
  - DevReq_L
- **Power per pin-pair is nil when in HyperTransport Device Stop mode**



PWROK, RESET_L required for proper reset & init
$V_{HyperTransport}$ routed between devices is required for proper common mode range

Bus Width (Each Way)	2	4	8	16	32
Data Pins (total)	8	16	32	64	128
Clock Pins (total)	4	4	4	8	16
Control Pins (total)	4	4	4	4	4
Subtotal (high speed)	**16**	**24**	**40**	**76**	**148**
VLDT	2	2	3	6	10
GND	4	6	10	19	37
PWROK	1	1	1	1	1
RESET_L	1	1	1	1	1
Total Pins	**24**	**34**	**55**	**103**	**197**
Total Max BW GB/s	0.8	1.6	3.2	6.4	12.8

DC Power per Pin-Pair: **4 - 9 mW, 6 $mW_{Typical}$**
Signal to V_{HT}/Gnd Ratio: **4:1**

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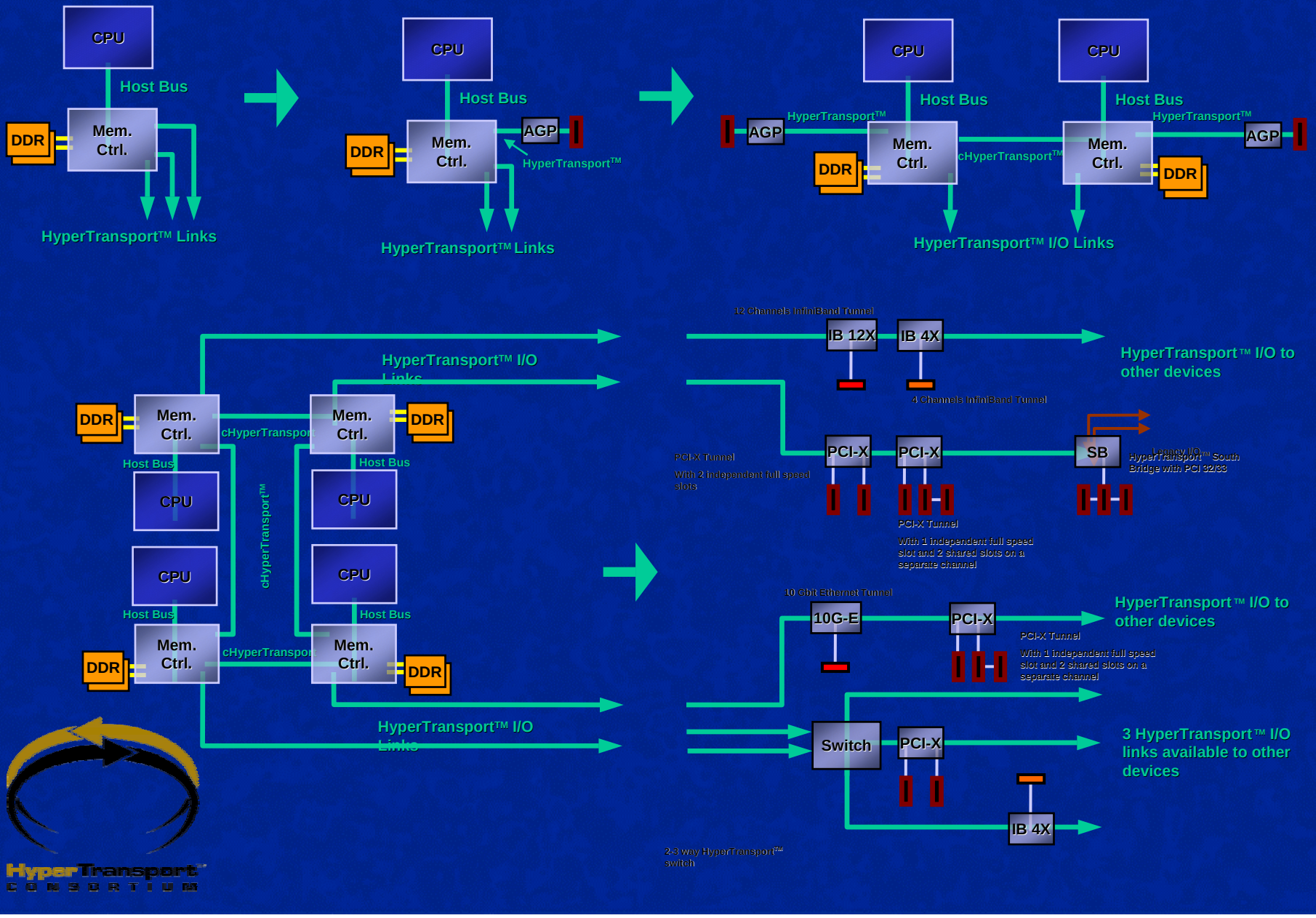
Possible Implementations in computers



HyperTransport™ Technology Vs serial links

- **Multiple GBytes/sec required**
  - A single wire clock+data at 10 Gbit/sec is only 1 GByte/sec or less. Not enough
- **Limits of FR4 material**
- **Embedded Clock efficiency**
  - A single wire clock+ data signaling may lose 5 to 25% efficiency* due to the embedded clock BW occupation
  - With multiple “bundled” wires 5% to 25% efficiency lost* on EACH wire, huge waste of silicon with clock recovery each individual wire
- **Now Vs Later**
  - PCI-X and InfiniBand are complementary to the HyperTransport™ technology
  - HyperTransport™ Silicon existing now
  - Technology endorsed by AMD,API,APPLE,Cisco,PMC-Sierra, Nvidia,Sun, Transmeta

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* 5 to 25% is the typical bandwidth assigned to the embedded clock in common implementation of similar speed in order to have enough information for the clock recovery mechanism and a reasonable balance in gate count.

Applications for HyperTransport™ Technology

- Routers
- Hubs
- Switches
- Servers
- Workstations
- PCs (Desktop & Notebook)
- Set-Top Boxes
- Mobile/Handheld Devices
- Game Consoles
- Embedded Systems

Any application requiring high-speed, low-latency and scalability!

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HyperTransport™ Technology Milestones

- First public presentation on HyperTransport™ Technology at Microprocessor Forum 99.
- Operational specification version 1.0 finished in May 2000. AMD distributes under NDA.
- HyperTransport Technology presentation with technical information at WinHEC 2000.
- HyperTransport Technology white paper becomes available early 2000 by AMD.
- HyperTransport Technology presentation at Platform 2000 (June 2000).
- 100+ companies evaluating spec and several licensing technology through AMD (2000).
- HyperTransport Technology Consortium officially launched July 23, 2001.
- First HyperTransport technology-based south bridge announced by NVIDIA (June 2001).
- Sibyte (Broadcom) announced its MIPS CPU with HyperTransport technology.
- Sandcraft announced its HyperTransport technology roadmap.
- Altera first FPGA family in Q1 2001.
- Teradyne and Dolphin Technology announce first test equipment for HyperTransport Technology (May 2001).
- Multiple HyperTransport technology-based chipsets for AMD Athlon™ processors in 2001.
- HyperTransport technology-based products are planned from AMD in 2002.

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HyperTransport™ Technology Consortium

- Incorporated as non-profit corporation and officially announced 7/24/2001
- Manages and controls the development and evolution of the specification
- Widespread support planned in networking, telecommunications, computers and embedded system companies
- Members have access to technical specifications and may participate in Consortium meetings and events
- Two membership levels are available: Contributor and Adopter
- To become a member, visit www.hypertransport.org
- Charter Members comprise the Executive Committee and include…

AMD · Api NetWorks · Cisco Systems · Sun microsystems (We're the dot in .com™) · PMC-Sierra (Making Global Networks Work) · NVIDIA · Transmeta

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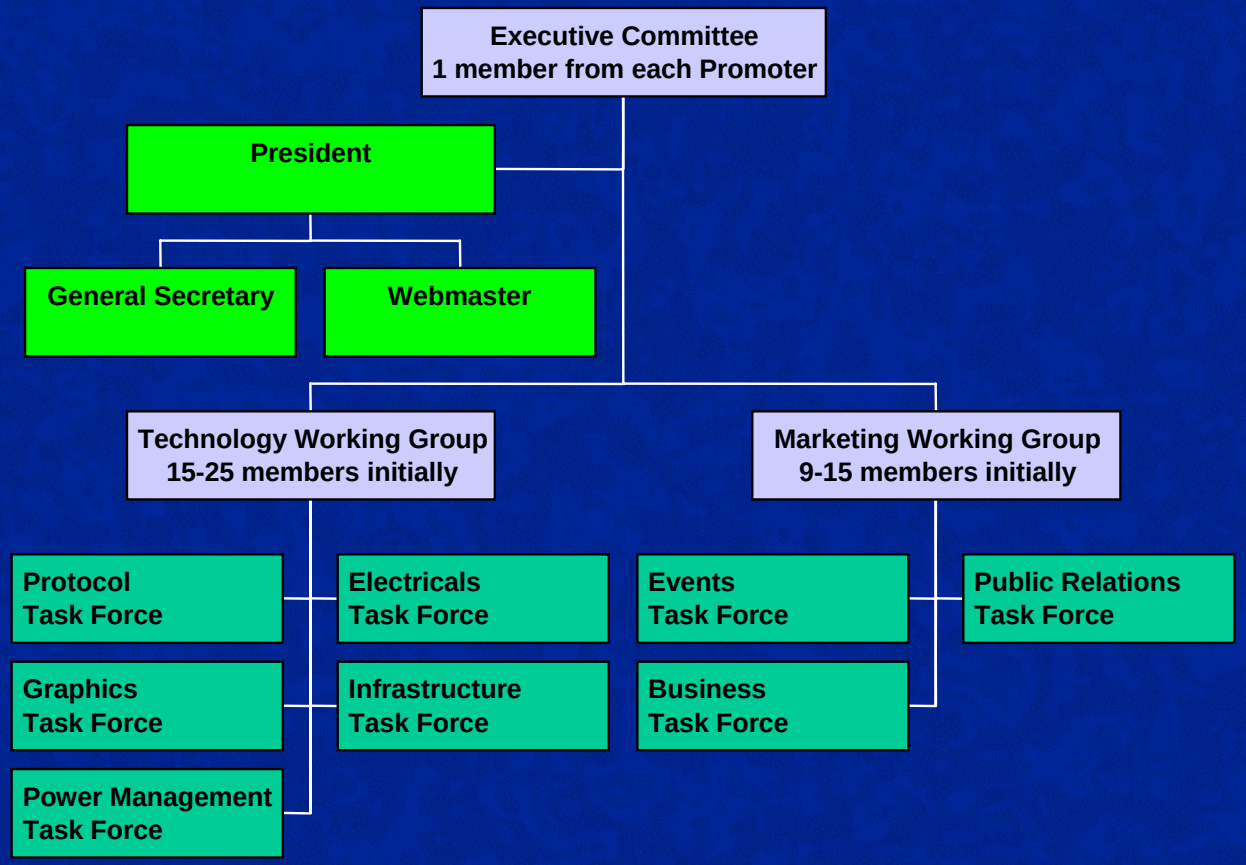
Consortium Structure



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Working Groups

- **Size is determined by the Executive Committee**
- **Contributors and Promoter will participate to the Working Groups**
- **Chairperson appointed by Executive Committee**
- **Working Groups create and staffs Task Forces**
  - appoints the Task Force chairperson
  - sets operating rules for Task Force
- **Supervises activities of subordinate Task Forces**
- **Reviews and approves proposals of Task Forces**
- **Presents all proposals to Executive Committee**
  - reports why proposals were approved or defeated

Technical Working Group

- **Target: 15-25 Voting Members,**
- **3+ from each Task Force**
- **Initially Proposed Task Forces:**
  - Protocol Task Force
  - Electricals Task Force
  - Graphics Task Force
  - Infrastructure Task Force
  - Power Management Task Force

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Protocol Task Force

- **Responsible for the editorial management of the *HyperTransport™ I/O Link Specification***
  - Today v1.02 available from AMD
  - Consortium plans to formally release v1.03 when completed

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Electricals Task Force

- **Has responsibility for editorial management of the *HyperTransport™ Technology Electrical Specification***
  - AMD will release v1.00 to consortium
  - Consortium plans to formally release v1.01 when completed
- **Potential activities**
  - promote migration of HyperTransport physical interfaces into common industry processes and standard cell libraries
  - adapt specifications to evolving manufacturing technologies
  - develop specification for HyperTransport over fiber
  - define a HyperTransport connector or family of connectors
  - investigate short distance rack-to-rack cabling solutions

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Graphics Task Force

- **Promote development of graphics bridges**
  - HyperTransport-to-AGP tunnels
  - Southbridge graphics
- **Investigate potential need for more graphic BW in desktop/workstation applications**

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Infrastructure Task Force

- **Promote the creation of HyperTransport™ Technology tools for design, debug, and verification**
- **Drive the availability of RTL cores, PHYs, models, and verification suites**
- **Promote the development of HyperTransport™ Technology diagnostics and compatibility tests**
- **Promote software solutions for HyperTransport™ Technology devices**
  - power mgmt, system mgmt, security, error recovery
- **Form a HyperTransport™ Technology standard compliance program**

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Power Management Task Force

- Create and evolve power management specifications
- Define docking and plugging requirements
- Promote “down-scaling” feature set
  - very low cost implementations
  - “narrow” and small form factor implementations
  - set very low voltage requirements

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Marketing Working Group

- **Target: 9 - 15 Voting Members**
- **3+ from each Task Force**
- **Initial Task Forces**
  - Events Task Force
  - Promotions and PR Task Force
  - Business Task Force

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Summary

- **HyperTransport™ Technology is an innovative technology that is designed to enable chips inside of PCs, networking and communications devices like those that power the Internet, to communicate with each other up to 24 times faster than existing technologies.**
- **Newly formed HyperTransport™ Technology Consortium is helping to drive HyperTransport™ technology to market.**
  - Consortium incorporated and announced July 23, 2001.
  - Industry heavyweights comprise the Consortium's Executive Committee – AMD, API NetWorks, Apple Computer, Cisco Systems, NVidia, PMC-Sierra, Sun Microsystems, Transmeta.
- **Consortium members announce that products using HyperTransport™ Technology are planned to ship later in 2001**